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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/622,835 | PAPPALARDO ET AL. | |
| | Examiner | Art Unit | |
| | James Sugent | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1-7 and 19-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Janssens et al. (U.S. Patent No. 6,122,751) and Neff (U.S. Patent No. 6,956,432 B2).

As per **claim 1**, Janssens et al discloses pipeline structure for use in a digital system, said pipeline structure comprising:

- a plurality of stages (Janssens et al discloses a pipeline circuit comprising four stages: the first stage [herein called STF] comprising a register 12a and combinatorial circuit 10a, stage two [herein called ST2] comprising a register 14 and combinatorial circuit 10b, stage three [herein called ST3] comprising a register 16 and combinatorial circuit 10c and the last stage [herein called STL] comprising a register 12b with no combinatorial circuit) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2, ST3) being interposed between the first stage and the last stage (column 3, lines 22-38); and

- a phase shifting circuit (18) for generating at least one local clock signal (18b and 18c) for controlling the at least one intermediate stage (ST2 and ST3; column 2, line 66 thru column 3, line 5),
- wherein the first stage (STF) and the last stage (STL) are controlled by the same clock signal (18a),
- the clock signal (18a) and the at least one local clock signal (18b and 18c) are out of phase (as shown in figure 2, 19a-c; column 3, lines 9-10).

Janssens et al fails to disclose a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.

Neff teaches a conventional interleaved clock generator (10) that is based on serial delay circuitry thus producing multiple clock signals (K1, K2, K3, K4) from a main clock (K0) with the same frequency but different phases (as shown in figure 3b; column 3, lines 23-42).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Janssens et al and Neff before him at the time the invention was made, to modify the clock-signaling scheme disclosed by Janssens et al to use the interleaved clock generator as taught by Neff wherein the main clock signal drives the first stage and the last stage and the produced clock signals to drive the intermediate stages.

One of ordinary skill in the art would be motivated to make use of an interleaved clock generator in view of the teachings of Neff, as doing so simplify the frequency aspects of the circuit design compared to those that use other techniques in the art to produce multi-phasing with the same frequency (Neff: column 4, lines 5-16).

As per **claim 2**, Janssens et al and Neff teach a pipeline structure,

- wherein the at least one intermediate stage comprising a plurality of intermediate stages (Janssens: ST2 and ST3 as defined above in claim 1),
- each of the intermediate stages is controlled by a corresponding local clock signal (Neff: K1 and K2) that is generated by the phase shifting circuit (Neff: 10), and
- the local clock signals are all out of phase with one another (Neff: as shown in figure 3b with K1 and K2; column 4, lines 5-17).

As per **claim 3**, Janssens et al and Neff teach a pipeline structure wherein for each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 1), the phase shifting circuit (Neff: 10) includes a delay block (Neff: 42-1, 42-2, 42-3 and 42-4) for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence (Neff: column 3, lines 31-42).

As per **claim 4**, Janssens et al and Neff teach a pipeline structure wherein each of the delay blocks (Neff: 42-1 and 42-2) produces the local clock signal (Neff: K1 and K2) for controlling the corresponding intermediate stage (Janssens: ST2 and ST3 as defined above in claim 1) from the clock signal controlling a next one of the stages in the sequence (Neff: column 3, lines 31-42).

As per **claim 5**, Janssens et al and Neff teach a pipeline structure wherein each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 1) includes a functional unit cascade (Janssens: combinatorial circuits 10b and 10c) connected to a buffer (Janssens: registers 14 and 16), the buffer storing an output of the functional unit of a previous one of the stages in the sequence based on the corresponding local clock signal (Janssens: column 3, lines 22-38), and the functional unit having a propagation time that is less than a phase difference between the corresponding local clock signal (Neff: K1 and K2) and the clock signal controlling the next one of the stages in the sequence (Neff: column 3, line 54 thru column 4, line 4; Janssens: column 2, line 66 thru column 3, line 5).

As per **claim 6**, Janssens discloses a pipeline structure wherein each of the functional units comprising a combinatorial circuit (combinatorial circuits 10b and 10c) and each of the buffers comprising a register for storing a word (registers 14 and 16; column 2, lines 57-65).

As per **claim 7**, Janssens and Neff teach a pipeline structure wherein for each of the at least one intermediate stages (Janssens: ST2 and ST3 as defined above in claim 1), the phase shifting circuit (Neff: 10) includes a delay block (Neff: 42-1 and 42-2) for producing the local clock signal (Neff: K1 and K2) controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence (Neff: column 3, line 54 thru column 4, line 4; Janssens: column 2, line 66 thru column 3, line 5).

As per **claim 19**, Janssens et al discloses a method of operating a pipeline structure that includes

- a plurality of stages (Janssens et al discloses a pipeline circuit comprising four stages: the first stage [herein called STF] comprising a register 12a and combinatorial circuit 10a, stage two [herein called ST2] comprising a register 14 and combinatorial circuit 10b, stage three [herein called ST3] comprising a register 16 and combinatorial circuit 10c and the last stage [herein called STL] comprising a register 12b with no combinatorial circuit) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2 and ST3) being interposed between the first stage and the last stage (column 3, lines 22-38), said method comprising the steps of:
- controlling the first stage (STF) and the last stage (STL) with the same clock signal (18a); and
- controlling the at least one intermediate stage (ST2 and ST3) with the at least one local clock signal (18b and 18c; column 2, line 66 thru column 3, line 5 ).

Janssens et al fails to disclose a method of operating a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.

Neff teaches a conventional interleaved clock generator (10) that is based on serial delay circuitry thus producing multiple clock signals (K1, K2, K3, K4) from a main clock (K0) with the same frequency but different phases (as shown in figure 3b; column 3, lines 23-42).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Janssens et al and Neff before him at the time the invention was made, to modify the clock-signaling scheme disclosed by Janssens et al to use the interleaved clock generator as taught by Neff wherein the main clock signal drives the first stage and the last stage and the produced clock signals to drive the intermediate stages.

One of ordinary skill in the art would be motivated to make use of an interleaved clock generator in view of the teachings of Neff, as doing so simplify the frequency aspects of the circuit design compared to those that use other techniques in the art to produce multi-phasing with the same frequency (Neff: column 4, lines 5-16).

As per **claim 20**, Janssens et al and Neff teach a method,

- wherein the at least one intermediate stage comprising a plurality of intermediate stages (Janssens: ST2 and ST3 as defined above in claim 19),
- in the generating step, one local clock signal is generated for each of the intermediate stages (Neff: K1 and K2),
- in the controlling step, each of the intermediate stages is controlled by a corresponding one of the local clock signals (Neff: column 3, line 54 thru column 4, line 4; Janssens: column 2, line 66 thru column 3, line 5).

As per **claim 21**, Neff teaches a method wherein the local clock signals (K1 and K2) are all out of phase with one another (as shown in figure 3b with K1 and K2; column 4, lines 5-17).

As per **claim 22**, Janssens et al and Neff teach a method wherein in the generating step, the local clock signal (Neff: K1 and K2) for each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 19) is generated from the clock signal controlling one of the stages that is adjacent in the sequence (Neff: column 3, lines 31-42).

As per **claim 23**, Janssens et al and Neff teach a method wherein in the generating step, the local clock signal (Neff: K1 and K2) for each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 19) is generated from the clock signal controlling a next one of the stages in the sequence (Neff: column 3, lines 31-42).

**Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Allen (U.S. Patent No. 5,909,638) and Janssens et al. (U.S. Patent No. 6,122,751).

As per **claim 8**, Allen discloses a digital system including at least one pipeline structure (parallel processing system 501: 501a, 501b...501c), the pipeline structure comprising:

- a plurality of stages (502, 504 and 506) arranged in a sequence from a first stage (502) for receiving an input (MPEG streams) of the pipeline structure to a last stage (506) for providing an output (to recorder) of the pipeline structure, with at least one intermediate stage (504) being interposed between the first stage and the last stage (as shown in figure 5; column 12, line 62 thru column 13, line 28).

Allen fails to disclose a digital system containing at least one pipeline structure wherein the pipeline structure comprises a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage.

Janssens et al teaches a pipeline structure comprising of a plurality of stages (Janssens et al teaches a pipeline circuit comprising four stages: the first stage [herein called STF] comprises a register 12a and combinatorial circuit 10a, stage two [herein called ST2] comprising a register 14 and combinatorial circuit 10b, stage three [herein called ST3] comprises a register 16 and combinatorial circuit 10c and the last stage [herein called STL] comprises a register 12b with no combinatorial circuit) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2, ST3) being interposed between the first stage and the last stage (column 3, lines 22-38); and a phase shifting circuit (18) for generating at least one local clock signal (18b and 18c) for controlling the at least one intermediate stage (ST2 and ST3; column 2, line 66 thru column 3, line 5), wherein the first stage (STF) and the last stage (STL) are controlled by the same clock signal (18a), the clock signal (18a) and the at least one local clock signal (18b and 18c) are out of phase (as shown in figure 2, 19a-c; column 3, lines 9-10).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Allen and Janssens et al before him at the time the invention was made, to modify the pipeline structures disclosed by Allen and use the pipeline structure as taught by Janssens wherein the pipeline structure contains a local clock circuit.

One of ordinary skill in the art would be motivated to make use of a pipeline structure with its own local clock in view of the teachings of Janssens, as doing so would reduce power consumption of the pipelined circuits without decreasing latency (Janssens: column 2, lines 3-5).

**Claims 8-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Allen (U.S. Patent No. 5,909,638) and Janssens et al. (U.S. Patent No. 6,122,751) as applied to claim 8 above, and further in view of Neff (U.S. Patent No. 6,956,423 B2).

As per **claim 8**, Allen and Janssens et al teach a digital system including at least one pipeline structure comprising:

- a plurality of stages (Janssens et al discloses a pipeline circuit comprising four stages: the first stage [herein called STF] comprising a register 12a and combinatorial circuit 10a, stage two [herein called ST2] comprising a register 14 and combinatorial circuit 10b, stage three [herein called ST3] comprising a register 16 and combinatorial circuit 10c and the last stage [herein called STL] comprising a register 12b with no combinatorial circuit) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2, ST3) being interposed between the first stage and the last stage (column 3, lines 22-38); and
- a phase shifting circuit (18) for generating at least one local clock signal (18b and 18c) for controlling the at least one intermediate stage (ST2 and ST3; column 2, line 66 thru column 3, line 5),
- wherein the first stage (STF) and the last stage (STL) are controlled by the same clock signal (18a),
- the clock signal (18a) and the at least one local clock signal (18b and 18c) are out of phase (as shown in figure 2, 19a-c; column 3, lines 9-10).

Allen and Janssens et al fail to teach a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.

Neff teaches a conventional interleaved clock generator (10) that is based on serial delay circuitry thus producing multiple clock signals (K1, K2, K3, K4) from a main clock (K0) with the same frequency but different phases (as shown in figure 3b; column 3, lines 23-42).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Allen, Janssens et al and Neff before him at the time the invention was made, to modify the clock-signaling scheme taught by Allen and Janssens et al to use the interleaved clock generator as taught by Neff wherein the main clock signal drives the first stage and the last stage and the produced clock signals to drive the intermediate stages.

One of ordinary skill in the art would be motivated to make use of an interleaved clock generator in view of the teachings of Neff, as doing so simplify the frequency aspects of the circuit design compared to those that use other techniques in the art to produce multi-phasing with the same frequency (Neff: column 4, lines 5-16).

As per **claim 9**, Allen, Janssens et al and Neff teach a digital system,

- wherein the at least one intermediate stage comprising a plurality of intermediate stages (Janssens: ST2 and ST3 as defined above in claim 8),
- each of the intermediate stages is controlled by a corresponding local clock signal (Neff: K1 and K2) that is generated by the phase shifting circuit (Neff: 10), and

- the local clock signals are all out of phase with one another (Neff: as shown in figure 3b with K1 and K2; column 4, lines 5-17).

As per **claim 10**, Allen, Janssens et al and Neff teach a digital system wherein for each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 8), the phase shifting circuit (Neff: 10) includes a delay block (Neff: 42-1, 42-2, 42-3 and 42-4) for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence (Neff: column 3, lines 31-42).

As per **claim 11**, Allen, Janssens et al and Neff teach a digital system wherein each of the delay blocks (Neff: 42-1 and 42-2) produces the local clock signal (Neff: K1 and K2) for controlling the corresponding intermediate stage (Janssens: ST2 and ST3 as defined above in claim 8) from the clock signal controlling a next one of the stages in the sequence (Neff: column 3, lines 31-42).

As per **claim 12**, Allen, Janssens et al and Neff teach a digital system wherein the digital system is a synchronous digital system (Allen: column 14, lines 57-63).

As per **claim 13**, Allen, Janssens et al and Neff teach a digital system wherein the digital system is a controller or microprocessor integrated in a chip (Allen discloses a video decompression engine 305 that controls the parallel processing circuits; column 12, line 62 thru column 13, line 12).

**Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,154,798) and Allen (U.S. Patent No. 5,909,638).

As per **claim 14**, Lin et al discloses an electronic device comprising a digital system (CPU 100) comprising a pipeline structure (column 5, lines 18-21) and a battery for supplying the digital system (column 4, lines 40-51).

Lin et al fails to disclose an electronic device wherein said digital system comprises the pipeline structure including: a plurality of stages arranged in a sequence from a first stage for receiving an input of the pipeline structure to a last stage for providing an output of the pipeline structure, with at least one intermediate stage being interposed between the first stage and the last stage, and the first stage and the last stage being controlled by a main clock signal; and a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage, the at least one local clock signal being generated from the main clock signal, and the main clock signal and the at least one local clock signal being out of phase.

Allen teaches a digital system including at least one pipeline structure (parallel processing system 501: 501a, 501b...501c), the pipeline structure comprising a plurality of stages (502, 504 and 506) arranged in a sequence from a first stage (502) for receiving an input (MPEG streams) of the pipeline structure to a last stage (506) for providing an output (to recorder) of the pipeline structure, with at least one intermediate stage (504) being interposed between the first stage and the last stage (as shown in figure 5; column 12, line 62 thru column 13, line 28).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Lin et al and Allen before him at the time the invention was made, to modify the digital system disclosed by Lin wherein the digital system comprises the parallel pipeline structure as taught by Allen.

One of ordinary skill in the art would be motivated to make use of a digital system with a parallel pipeline structure in view of the teachings of Allen, as doing so would allow for faster processing speeds during read/write instructions (Allen: column 3, lines 54-60).

**Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,154,798) and Allen (U.S. Patent No. 5,909,638) as applied to claim 14 above, and further in view of Janssens et al. (U.S. Patent No. 6,122,751).

As per **claim 14**, Lin et al and Allen teach an electronic device comprising:

- a digital system (Lin: CPU 100) including a pipeline structure (Lin: column 5, lines 18-21), the pipeline structure including:
- a plurality of stages (Allen: 502, 504 and 506) arranged in a sequence from a first stage (Allen: 502) for receiving an input (MPEG streams) of the pipeline structure to a last stage (Allen: 506) for providing an output (to recorder) of the pipeline structure, with at least one intermediate stage (Allen: 504) being interposed between the first stage and the last stage (Allen: as shown in figure 5; column 12, line 62 thru column 13, line 28); and
- a battery for supplying the digital system (Lin: column 4, lines 40-51).

Lin et al and Allen fail to teach an electronic device comprising a digital system containing at least one pipeline structure wherein the pipeline structure comprises a phase shifting circuit for generating at least one local clock signal for controlling the at least one intermediate stage.

Janssens et al teaches a pipeline structure comprising of a plurality of stages (Janssens et al teaches a pipeline circuit comprising four stages: the first stage [herein called STF] comprises a register 12a and combinatorial circuit 10a, stage two [herein called ST2] comprising a register 14 and combinatorial circuit 10b, stage three [herein called ST3] comprises a register 16 and combinatorial circuit 10c and the last stage [herein called STL] comprises a register 12b with no combinatorial circuit) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2, ST3) being interposed between the first stage and the last stage (column 3, lines 22-38); and a phase shifting circuit (18) for generating at least one local clock signal (18b and 18c) for controlling the at least one intermediate stage (ST2 and ST3; column 2, line 66 thru column 3, line 5), wherein the first stage (STF) and the last stage (STL) are controlled by the same clock signal (18a), the clock signal (18a) and the at least one local clock signal (18b and 18c) are out of phase (as shown in figure 2, 19a-c; column 3, lines 9-10).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Allen and Janssens et al before him at the time the invention was made, to modify the pipeline structures disclosed by Allen and use the pipeline structure as taught by Janssens wherein the pipeline structure contains a local clock circuit.

One of ordinary skill in the art would be motivated to make use of a pipeline structure with its own local clock in view of the teachings of Janssens, as doing so would reduce power consumption of the pipelined circuits without decreasing latency (Janssens: column 2, lines 3-5).

**Claims 14-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,154,798), Allen (U.S. Patent No. 5,909,638) and Janssens et al. (U.S. Patent No. 6,122,751) as applied to claim 14 above, and further in view of Neff (U.S. Patent No. 6,956,423 B2).

As per **claim 14**, Lin et al, Allen and Janssens teach an electronic device comprising:

- a digital system (Lin: CPU 100) including at least one pipeline structure (Allen: 502, 504 and 506), the pipeline structure including:
- a plurality of stages (Janssens: STF, STL, ST2 and ST3 as defined above in claim 14) arranged in a sequence from a first stage (STF) for receiving an input of the pipeline structure to a last stage (STL) for providing an output of the pipeline structure, with at least one intermediate stage (ST2 and ST3) being interposed between the first stage and the last stage (column2, lines 57-65), and the first stage and the last stage being controlled by the same clock signal (column 2, line 66 thru column 3, line 5); and
- a phase shifting circuit (Janssens: 18) for generating at least one local clock signal (Janssens: 18b and 18c) for controlling the at least one intermediate stage (ST2 and ST3), the at least one local clock signal being out of phase (Janssens: column 3, lines 9-16); and

- a battery for supplying the digital system (Lin: column 4, lines 40-51).

Lin et al, Allen and Janssens et al fail to teach a pipeline wherein the first stage (STF) and the last stage (STL) are controlled by a main clock such that local intermediate clock signals to drive the intermediate stages (ST2 and ST3) are generated from said main clock signal.

Neff teaches a conventional interleaved clock generator (10) that is based on serial delay circuitry thus producing multiple clock signals (K1, K2, K3, K4) from a main clock (K0) with the same frequency but different phases (as shown in figure 3b; column 3, lines 23-42).

It would have been obvious to one of ordinary skill of the art, having the teachings of the Lin et al, Allen, Janssens et al and Neff before him at the time the invention was made, to modify the clock-signaling scheme taught by Lin et al, Allen and Janssens et al to use the interleaved clock generator as taught by Neff wherein the main clock signal drives the first stage and the last stage and the produced clock signals to drive the intermediate stages.

One of ordinary skill in the art would be motivated to make use of an interleaved clock generator in view of the teachings of Neff, as doing so simplify the frequency aspects of the circuit design compared to those that use other techniques in the art to produce multi-phasing with the same frequency (Neff: column 4, lines 5-16).

As per **claim 15**, Lin et al, Allen, Janssens et al and Neff teach an electronic device,

- wherein the at least one intermediate stage of the pipeline structure of the digital system consists of a plurality of intermediate stages (Janssens: ST2 and ST3 as defined above in claim 14),

- each of the intermediate stages is controlled by a corresponding local clock signal (Neff: K1 and K2) that is generated by the phase shifting circuit (Neff: 10), and
- the local clock signals are all out of phase with one another (Neff: as shown in figure 3b with K1 and K2; column 4, lines 5-17).

As per **claim 16**, Lin et al, Allen, Janssens et al and Neff teach an electronic device wherein for each of the intermediate stages (Janssens: ST2 and ST3 as defined above in claim 14) of the pipeline structure of the digital system, the phase shifting circuit (Neff: 10) includes a delay block (Neff: 42-1, 42-2, 42-3 and 42-4) for producing the local clock signal controlling that intermediate stage from the clock signal controlling one of the stages that is adjacent in the sequence (Neff: column 3, lines 31-42).

As per **claim 17**, Lin et al, Allen, Janssens et al and Neff teach an electronic device wherein each of the delay blocks (Neff: 42-1 and 42-2) produces the local clock signal (Neff: K1 and K2) for controlling the corresponding intermediate stage (Janssens: ST2 and ST3 as defined above in claim 14) from the clock signal controlling a next one of the stages in the sequence (Neff: column 3, lines 31-42).

As per **claim 18**, Lin et al, Allen, Janssens et al and Neff teach an electronic device wherein the electronic device is a hand-held computer (Lin: laptop; column 1, lines 29-35 and column 4, lines 40-51) and the digital system is a controller or microprocessor of the hand-held computer

(Allen discloses a video decompression engine 305 that controls the parallel processing circuits; column 12, line 62 thru column 13, line 12).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

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